Digital Electronics.

CHAPTER THIRTY TWO

Semiconductor Read-Only Memories

Introduction

Diode circuits, BJT circuits, and MOSFET circuits are used to provide memory semiconductor circuits consisting of both Read-Only Memories (ROM) and Random-Access Memories (RAM) (*next chapter*).

Figure 1

© *http://computer.howstuffworks.com/rom4.htm*

ROM chips (Figure 1) contain a grid of columns and rows. But where the columns and rows intersect, ROM chips are fundamentally different from RAM chips. While RAM uses transistors to turn on or off access to a capacitor at each intersection, ROM uses a **diode** to connect the lines if the value is 1. If the value is 0, then the lines are not connected at all.

Ch. 32

Introduction

Semiconductor IC ROMs refer to sub-circuits that are designed to store a predefined pattern of values in a binary format by encoding each logic "0" and "1" by the absence or presence of a single diode or transistor.

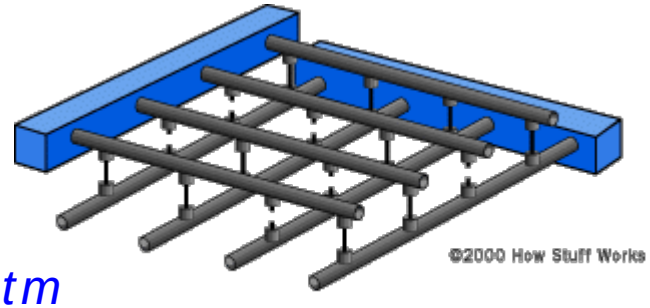
Entire chips can be designed as ROMs to store a program such as the boot up code and basic input/output service (BIOS) routines used by computers.

IC ROMs can be used to store operating software for appliances such as microwave ovens, washing machines

Introduction

Special types of ROMs can be programmed after fabrication (Programmable Read-Only Memory (PROM). In PROMs, a fuse is connected with a diode or a transistor. So the PROMs can be programmed by intentionally blowing the fuse of each bit that is desired to be inverted.

Figure 2



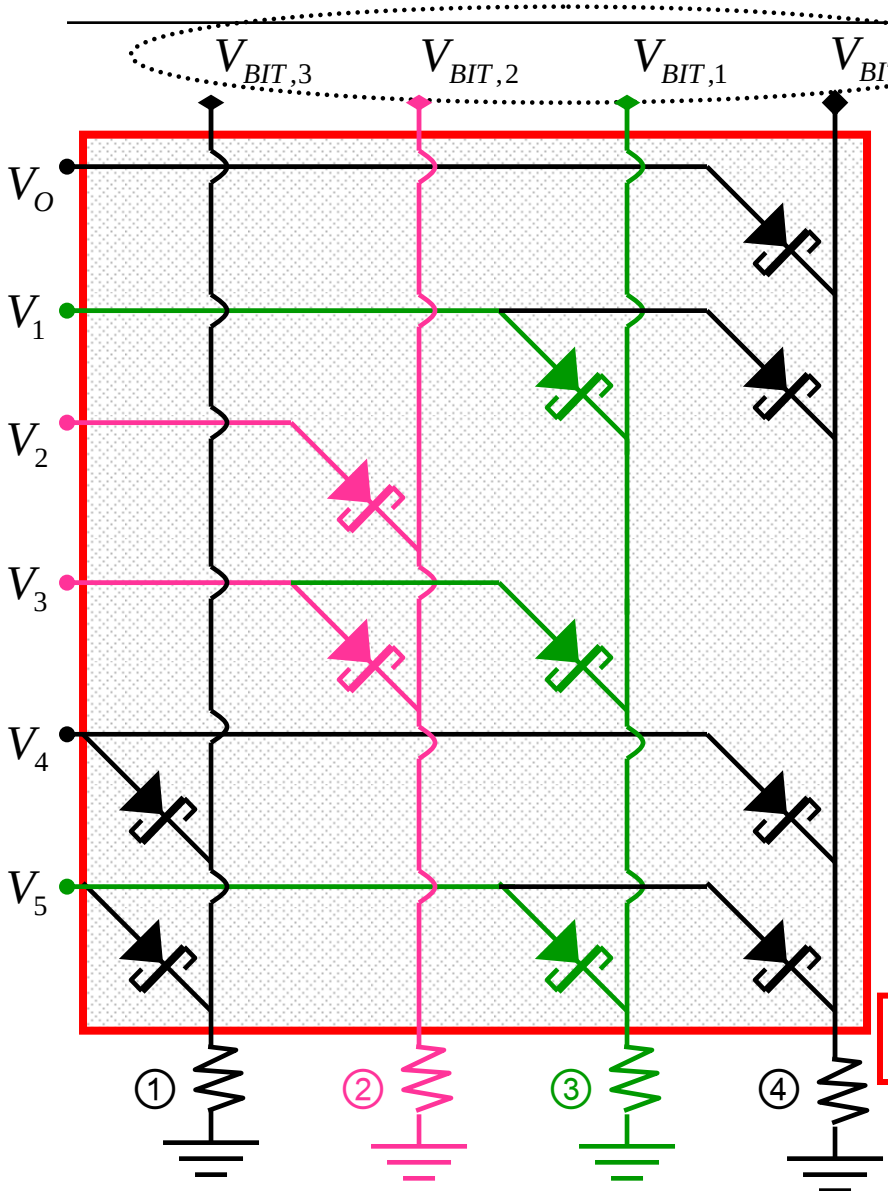
PROM

http://computer.howstuffworks.com/rom3.htm

PROM chips (Figure 2) have a grid of columns and rows just as ordinary ROMs do. The difference is that every intersection of a column and row in a PROM chip has a fuse connecting them. A charge sent through a column will pass through the fuse in a cell to a grounded row indicating a value of 1. Since all the cells have a fuse, the initial (blank) state of a PROM chip is all 1s. To change the value of a cell to 0, you use a programmer to send a specific amount of current to the cell. The higher voltage breaks the connection between the column and row by burning out the fuse. This process is known as burning the PROM.

PROMs can only be programmed once.

Diode Read-Only Memories

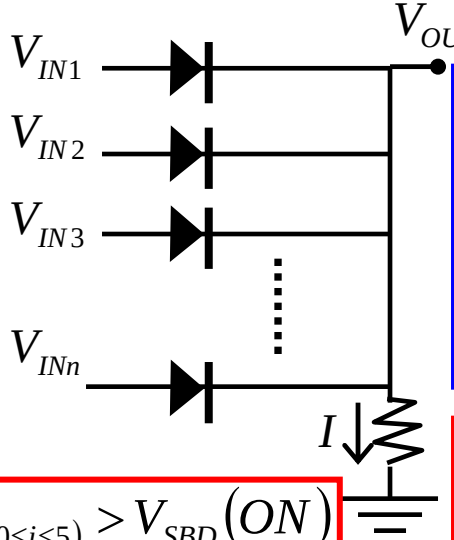


①: 2-input diode OR gate V_4 V_5

②: 2-input diode OR gate V_2 V_3

③: 3-input diode OR gate V_1 V_3 V_5

④: 4-input diode OR gate V_O V_1 V_4 V_5



With all inputs low ($<V_{D(ON)}$), all diodes are off, → I=0, $V_{OUT}=0$.

With one input high ($>V_{D(ON)}$), → $I \neq 0$, $V_{OUT}=V_{CC}-V_{D(ON)}$.

$$V_{i(0\le i\le 5)} > V_{SBD}(ON)$$

$$V_{SBD}(ON) = 0.3V$$

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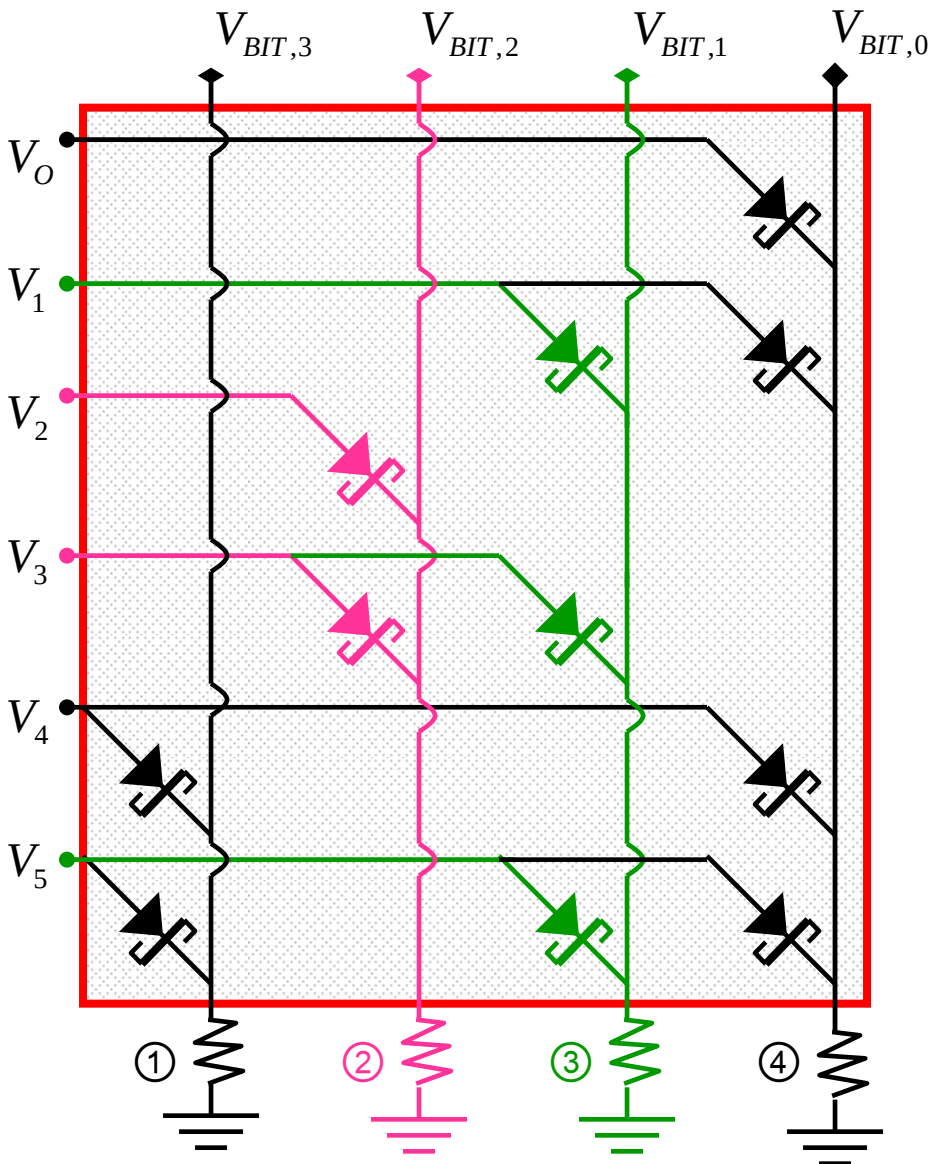
Diode Read-Only Memories



- This circuit (*Schottky diode ROM*) represents a simple four bit, six address ROM cell

- The data out bit lines are labeled

  $V_{BIT,3}$ $V_{BIT,2}$ $V_{BIT,1}$ $V_{BIT,0}$

- In all CMOS ROM circuits, a high voltage is regarded as a **1** and a low voltage as a **0**.

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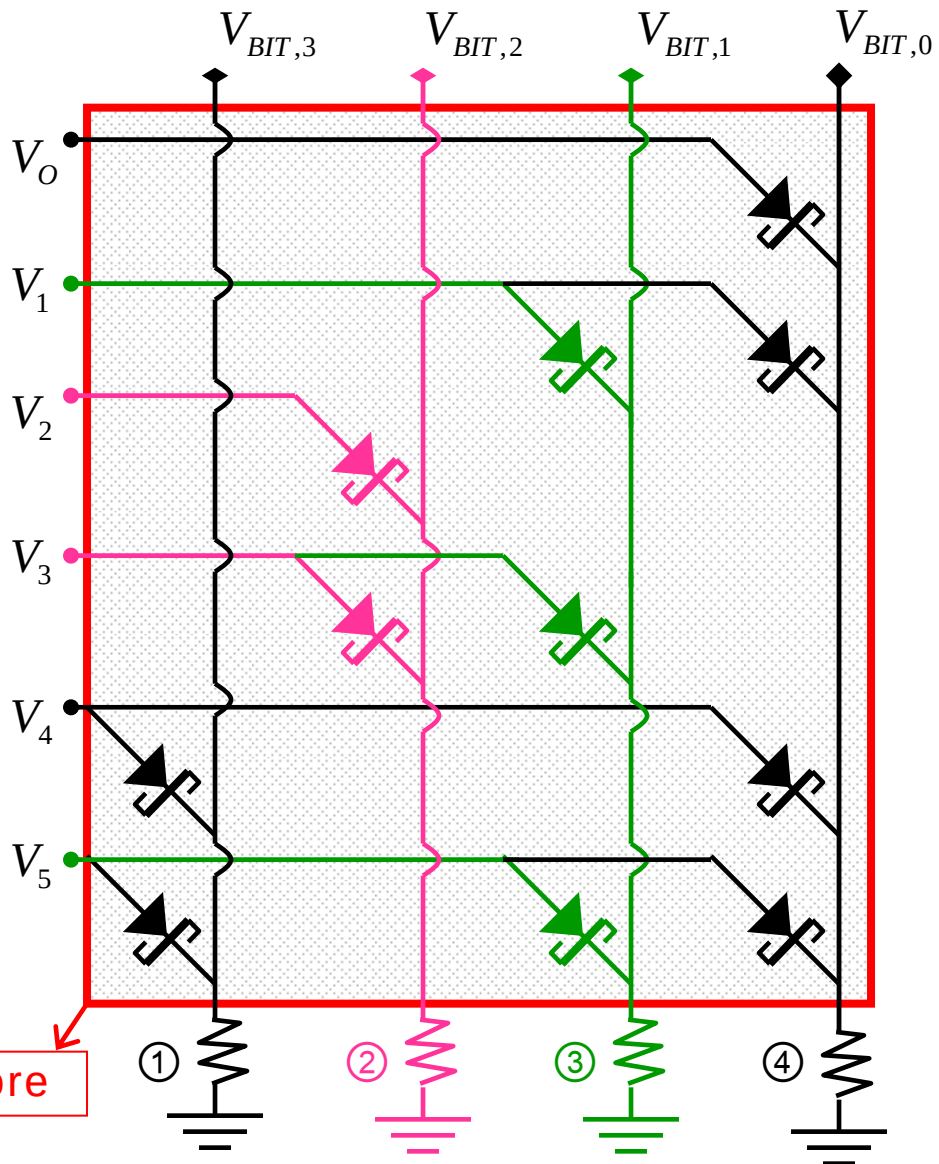
Operation of Diode ROM



Only V_O is high "1"

Data Output values: **0001**

Only V_1 is high "1"

Data Output values: **0011**

Only V_2 is high "1"

Data Output values: **0100**

Only V_3 is high "1"

Data Output values: **0110**

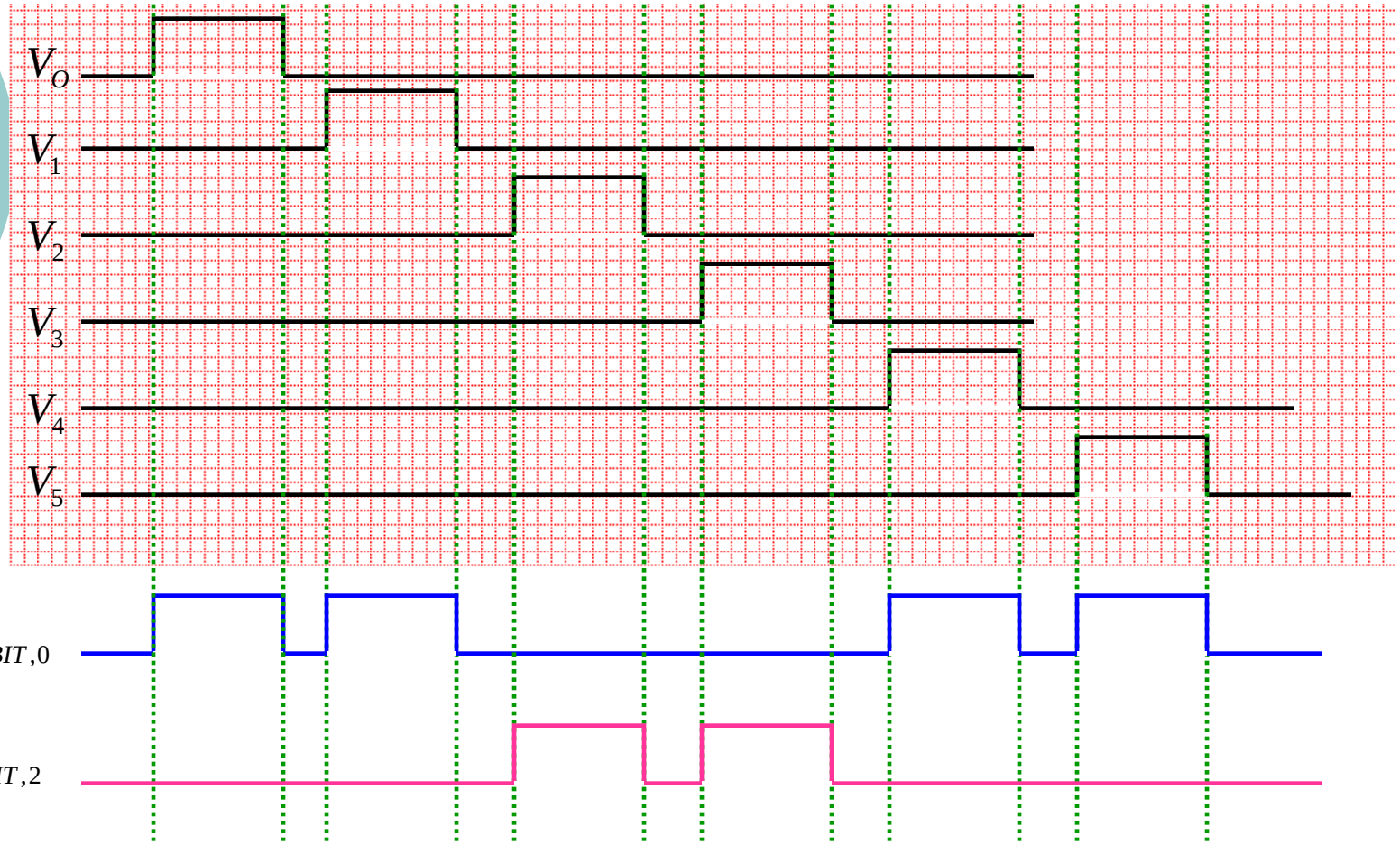
Only V_4 is high "1"

Data Output values: **1001**

Only V_5 is high "1"

Data Output values: **1011**

Utilization of Diode ROM Circuit



④: 4-input diode OR gate V_O V_1 V_4 V_5

②: 2-input diode OR gate V_2 V_3

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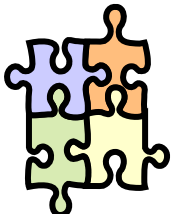
Design of Diode ROM Circuit

- Diodes are to be placed between input row lines and data out column lines where logic high bits are desired.

- An absence of a diode stores logic low



Example

Design a Shottky diode ROM circuit that has five data out bits and stores the six decimal (basis 10) values 21,14,1,10, 13, and 18

Solution

The diode ROM circuit stores binary values (decimal→ binary)

$(21)_{10} = 16+4+1 = 2^4+2^2+2^0 \rightarrow (\mathbf{10101})_2$

$(14)_{10} = 8+4+2 = 2^3+2^2+2^1 \rightarrow (\mathbf{01110})_2$

$(1)_{10} = 1 = 2^0 \rightarrow (\mathbf{00001})_2$

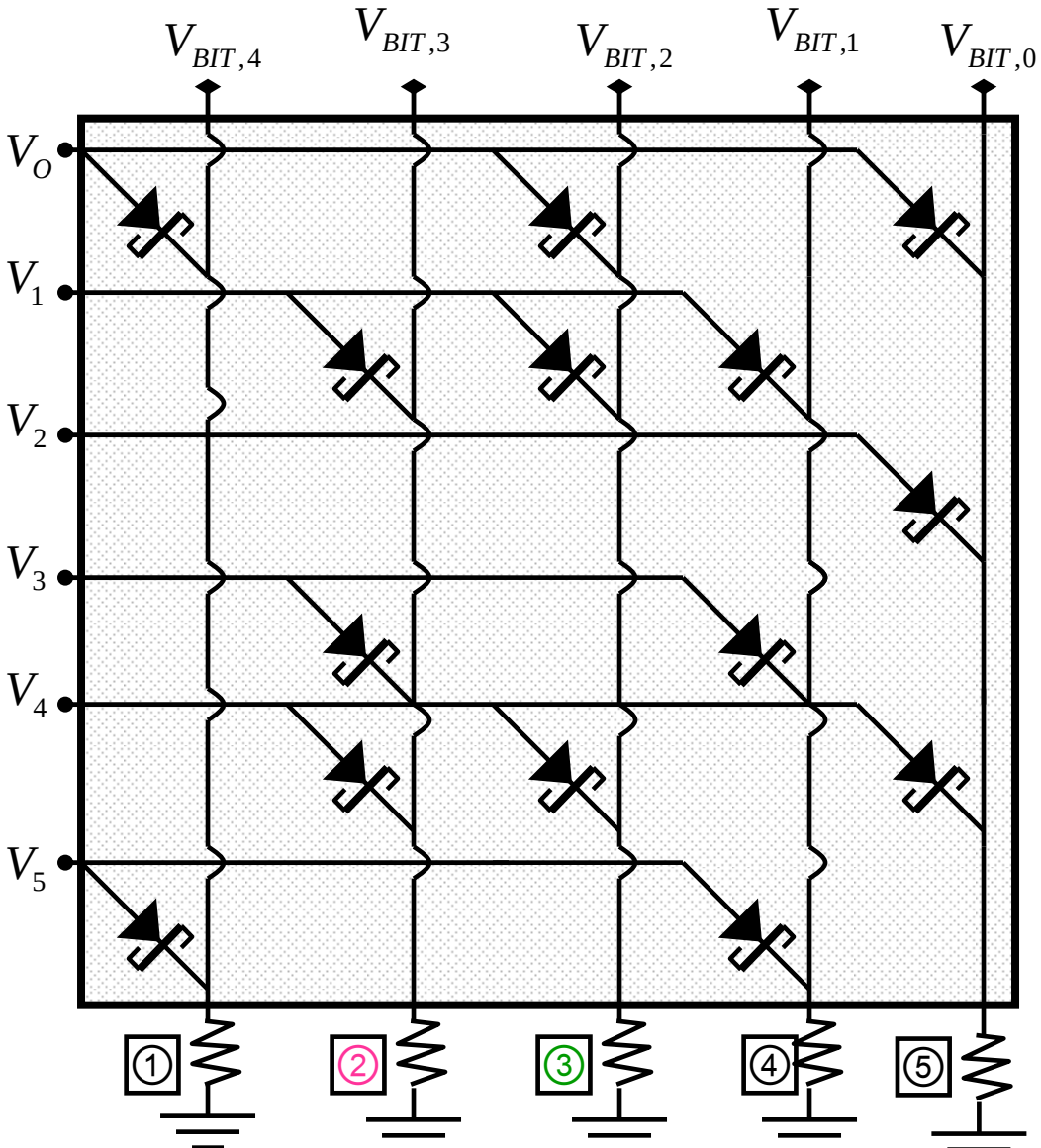
$(10)_{10} = 8+2 = 2^3+2^1 \rightarrow (\mathbf{01010})_2$

$(13)_{10} = 8+4+1 = 2^3+2^2+2^0 \rightarrow (\mathbf{01101})_2$

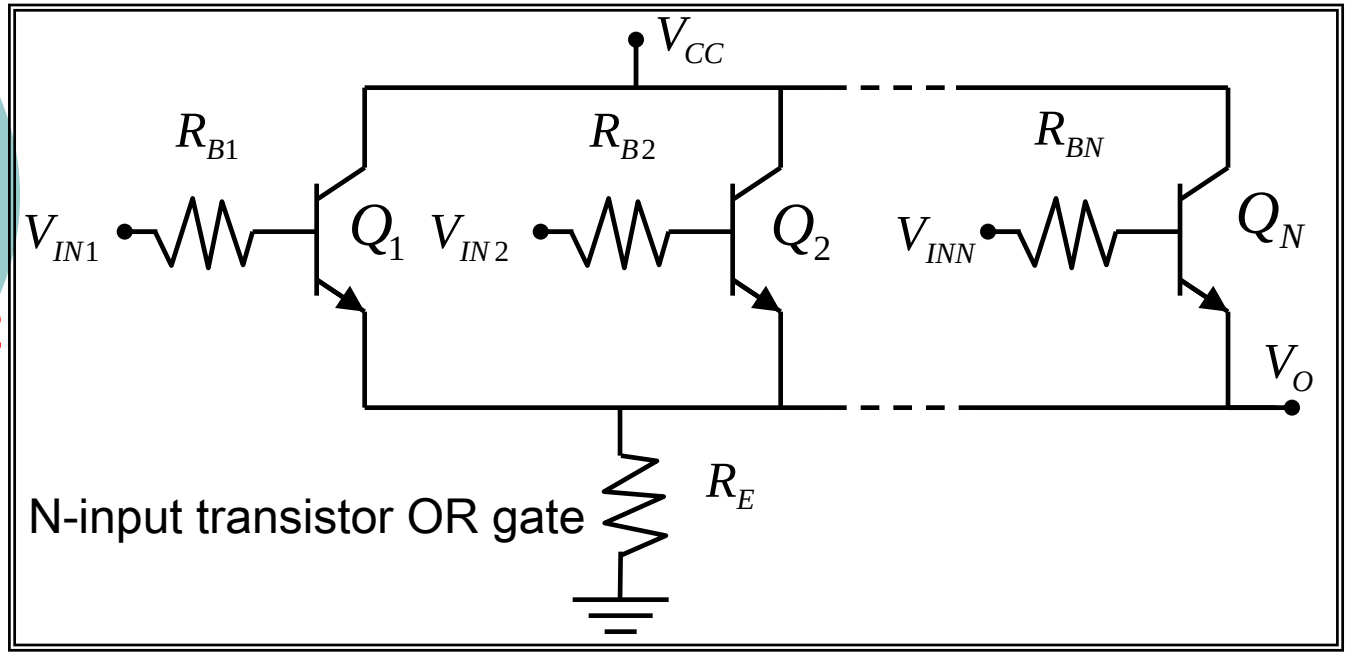
$(18)_{10} = 16+2 = 2^4+2^1 \rightarrow (\mathbf{10010})_2$

- Solution

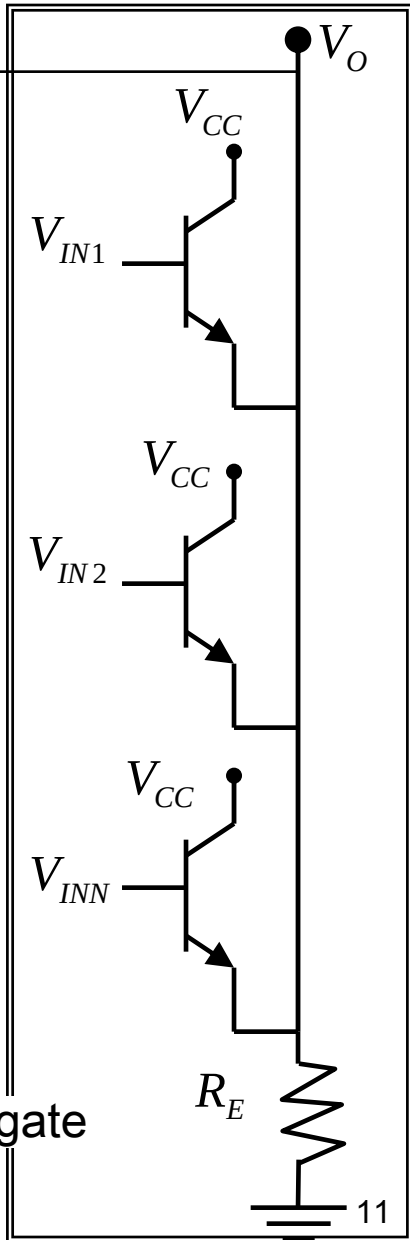
V0→$(\mathbf{10101})_2$
V1→$(\mathbf{01110})_2$
V2→$(\mathbf{00001})_2$
V3→$(\mathbf{01010})_2$
V4→$(\mathbf{01101})_2$
V5→$(\mathbf{10010})_2$



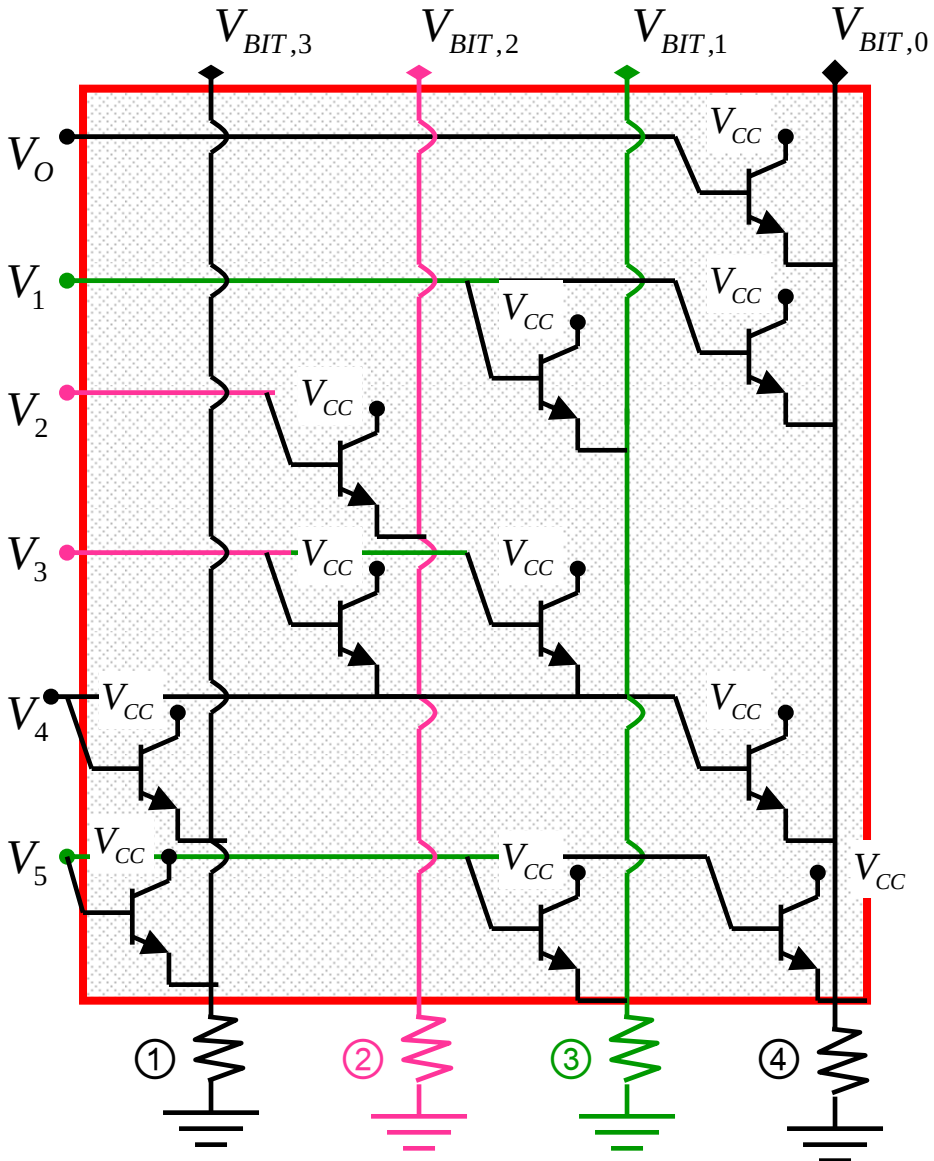
BJT Read-Only Memories



- The *Schottky diodes are replaced by BJTs*



BJT Read-Only Memories

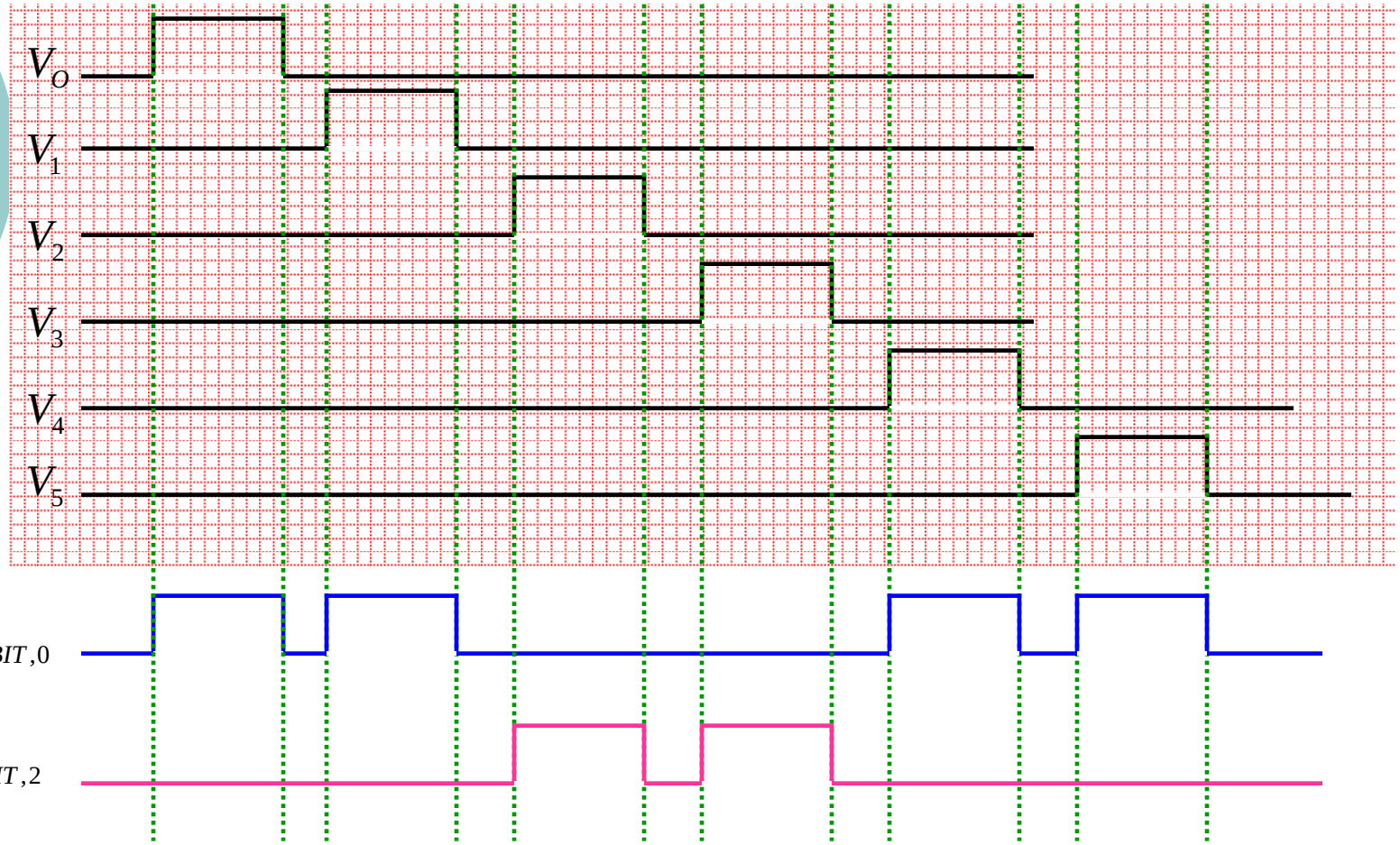


- This circuit (*BJT ROM*) represents a simple four bit, six address ROM cell

- The data out bit lines are labeled

$V_{BIT,3}$ $V_{BIT,2}$ $V_{BIT,1}$ $V_{BIT,0}$

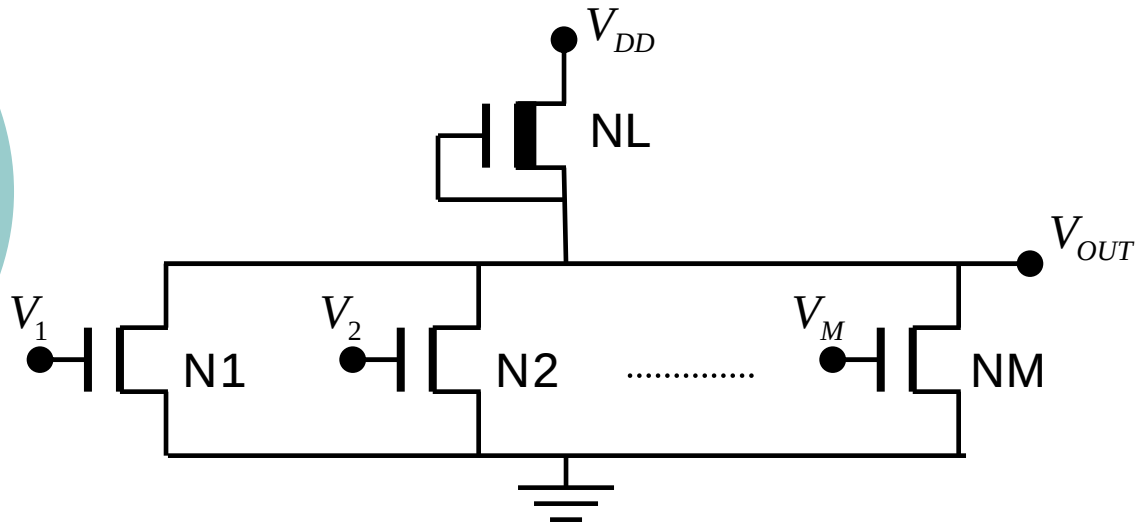
Utilization of BJT ROM Circuit



④: 4-input BJT OR gate V_O V_1 V_4 V_5

②: 2-input BJT OR gate V_2 V_3

NMOS Read-Only Memories



$$V_{OH} = V_{DD} - V_L(OH)$$

$$V_L(OH) = 0$$

- The NOR gate with at least one high-input has a low output logic level.
- The NOR gate with all its inputs are low has a high output logic level.

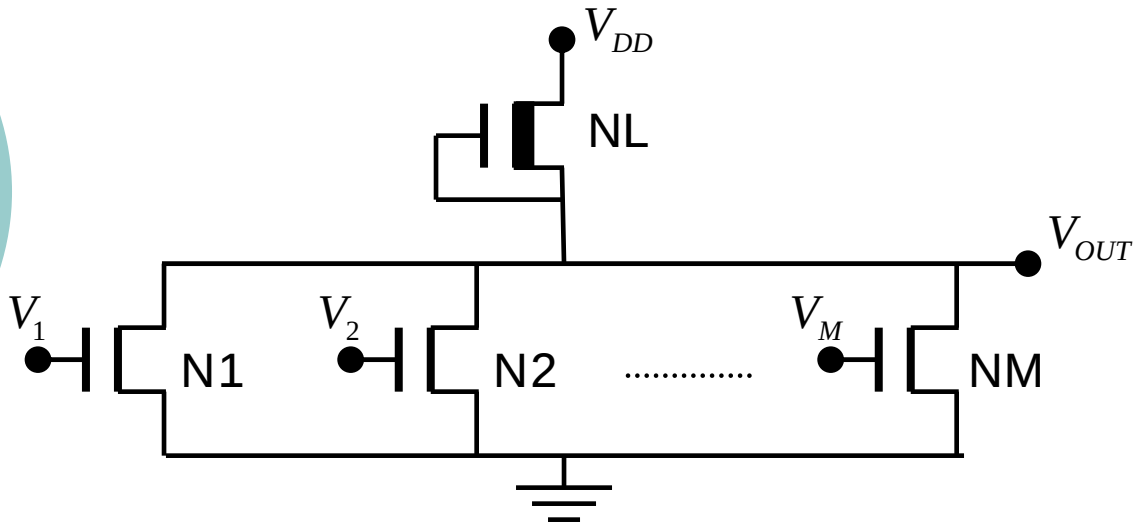
For all NMOS logic families except the saturated enhancement-only loaded NMOS

$$V_{OL}(\text{E} - \text{D loaded}) = \frac{k_L V_{T,L}^2}{2k_O(V_{DD} - V_{T,O})}$$

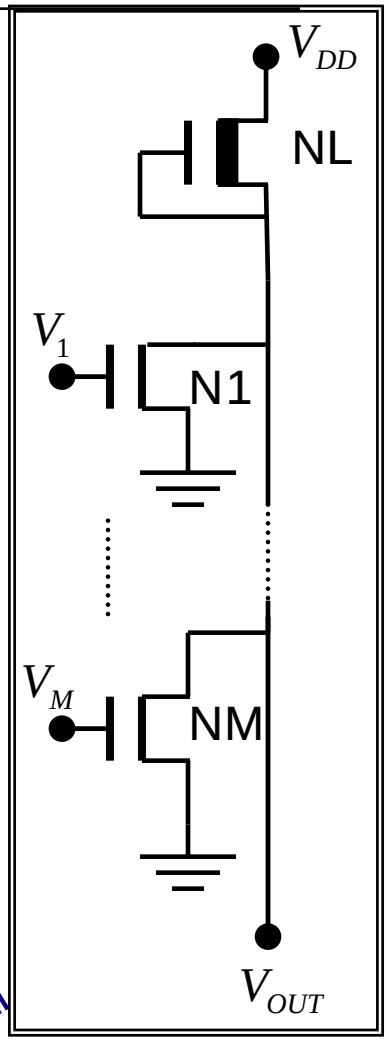
$$k_O = \mu_n C_{ox}\left(\frac{W_{O,1}}{L_{O,1}} + \frac{W_{O,2}}{L_{O,2}} + \cdots \frac{W_{O,M}}{L_{O,M}}\right)$$

Transconductance parameter

NMOS Read-Only Memories



M-input NMOS NOR gate



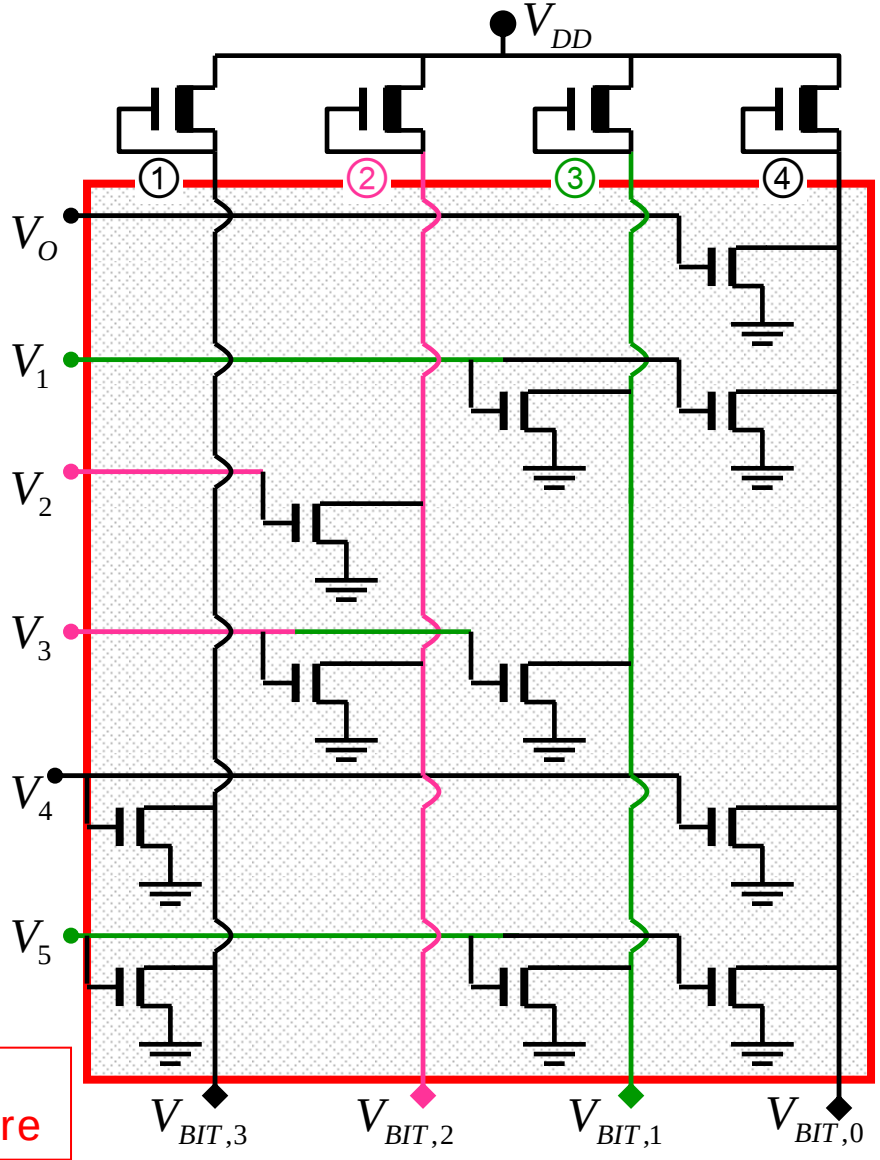
Each enhancement NMOS provides an output pull-down path

The single depletion NMOS provides an output pull-up path

$$V_{GS,L} = 0 > V_{TN,L} \Rightarrow ON$$

Basis of NMOS ROM cell

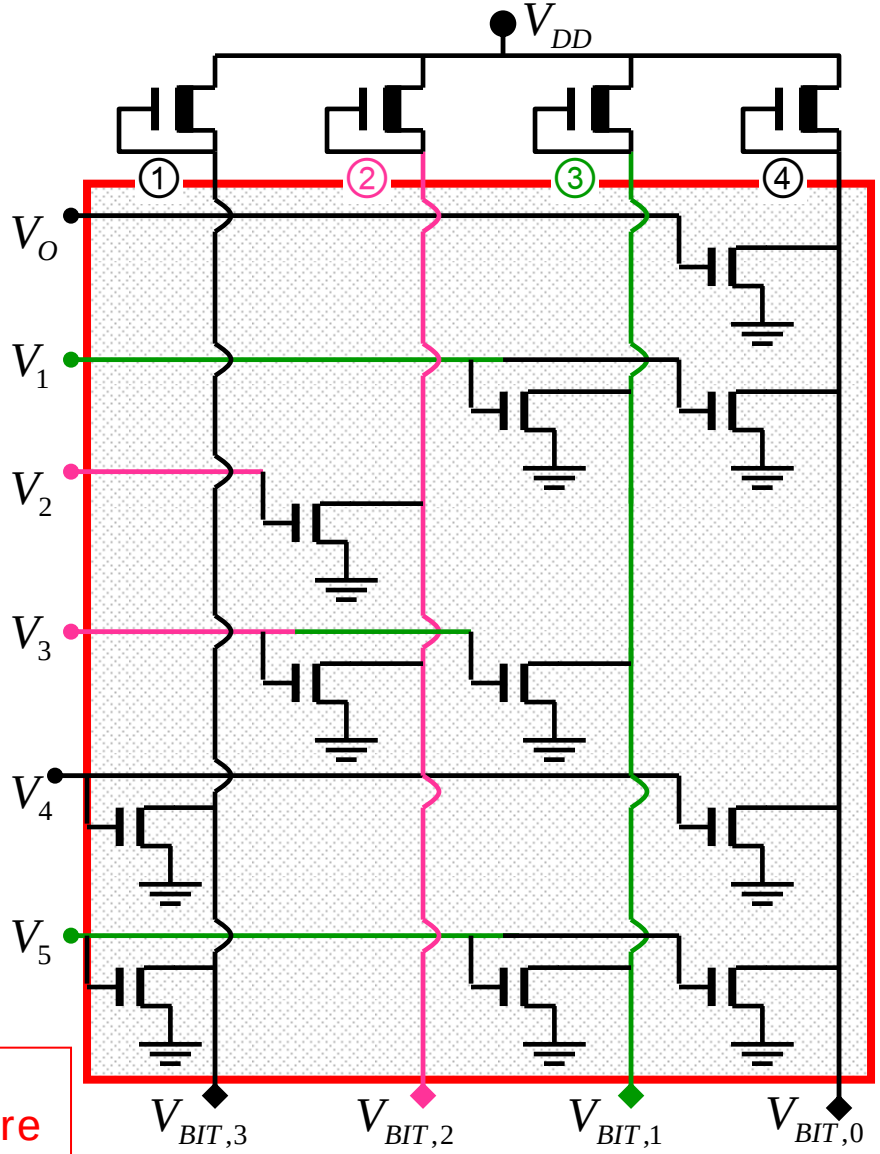
Operation of NMOS NOR ROM Cell



- This circuit (*NMOS ROM*) represents a simple four bit, six address ROM cell
- The data out bit lines are labeled

  $V_{BIT,3}$ $V_{BIT,2}$ $V_{BIT,1}$ $V_{BIT,0}$
- The NOR gate with at least one high-input has a low output logic level.
- The NOR gate with all its inputs are low has a high output logic level.

Operation of NMOS NOR ROM Cell



NMOS ROM Core

Only V_O is high "1"

Data Output values: **1110**

Only V_1 is high "1"

Data Output values: **1100**

Only V_2 is high "1"

Data Output values: **1011**

Only V_3 is high "1"

Data Output values: **1001**

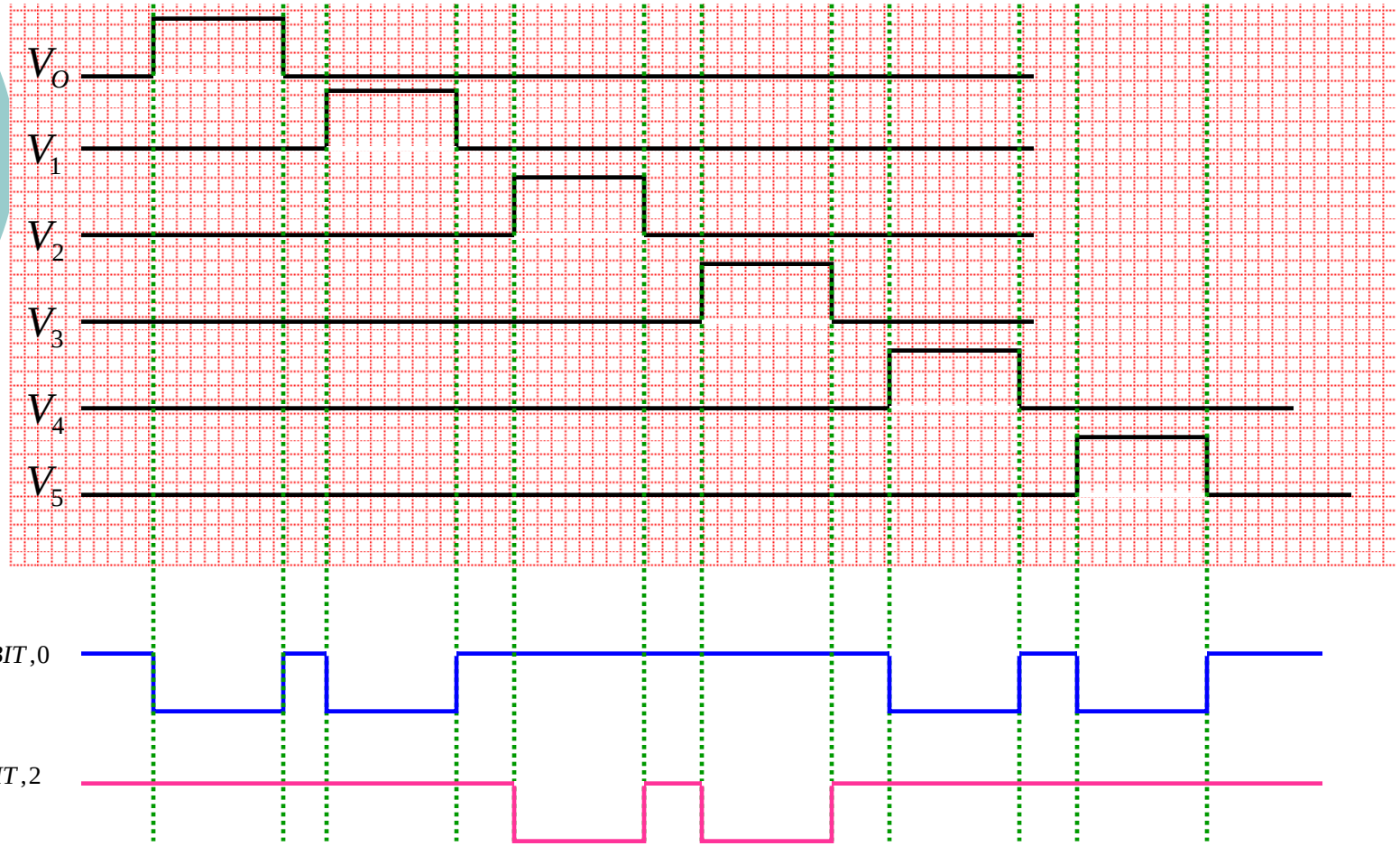
Only V_4 is high "1"

Data Output values: **0110**

Only V_5 is high "1"

Data Output values: **0100**

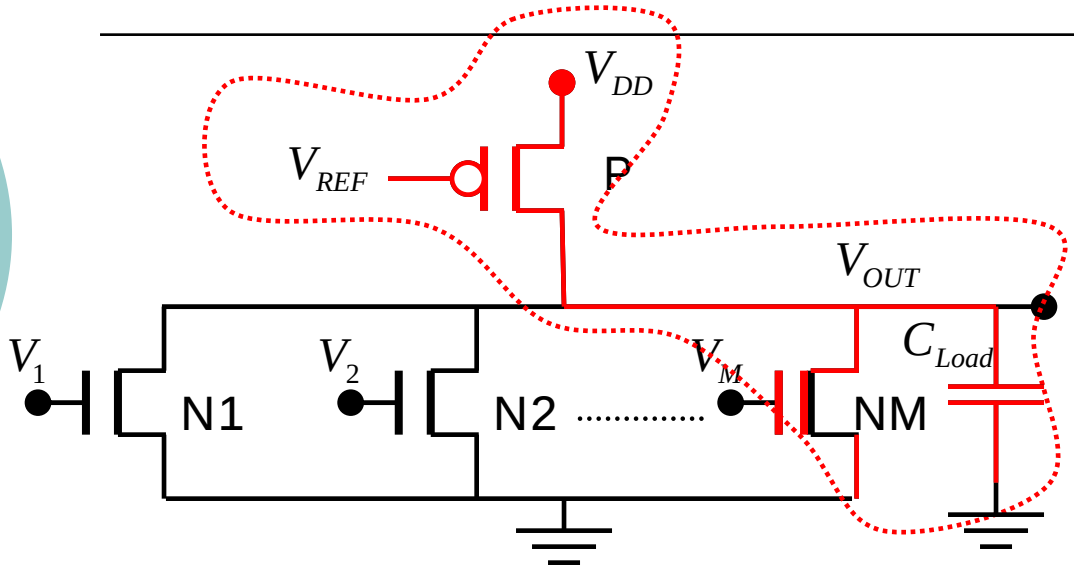
Utilization of NMOS NOR ROM Cell

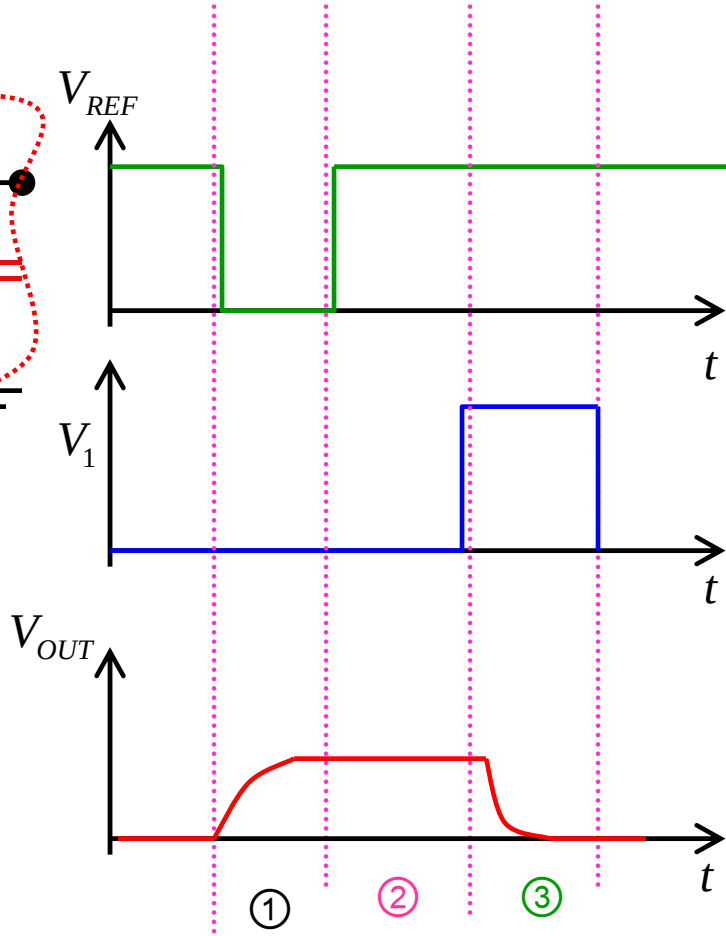


④: 4-input NMOS NOR gate V_O V_1 V_4 V_5

②: 2-input NMOS NOR gate V_2 V_3

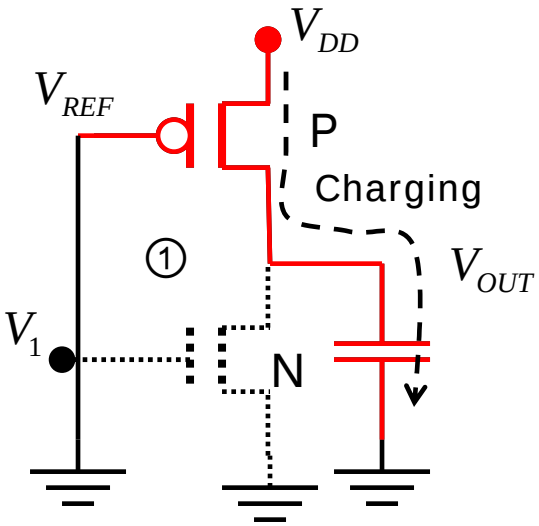
CMOS Read-Only Memories

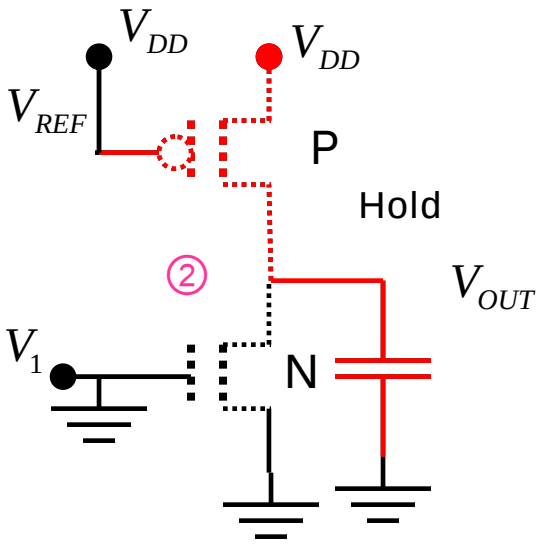


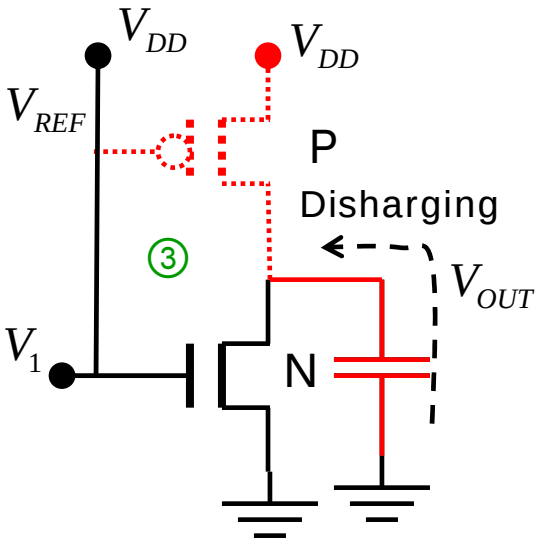


- Unlike the previous ROMs, the CMOS output depends on the storage of charge in the load capacitance on each bit output line.
- To have a zero power consumption
- The CMOS ROMs dissipate power only during switching.

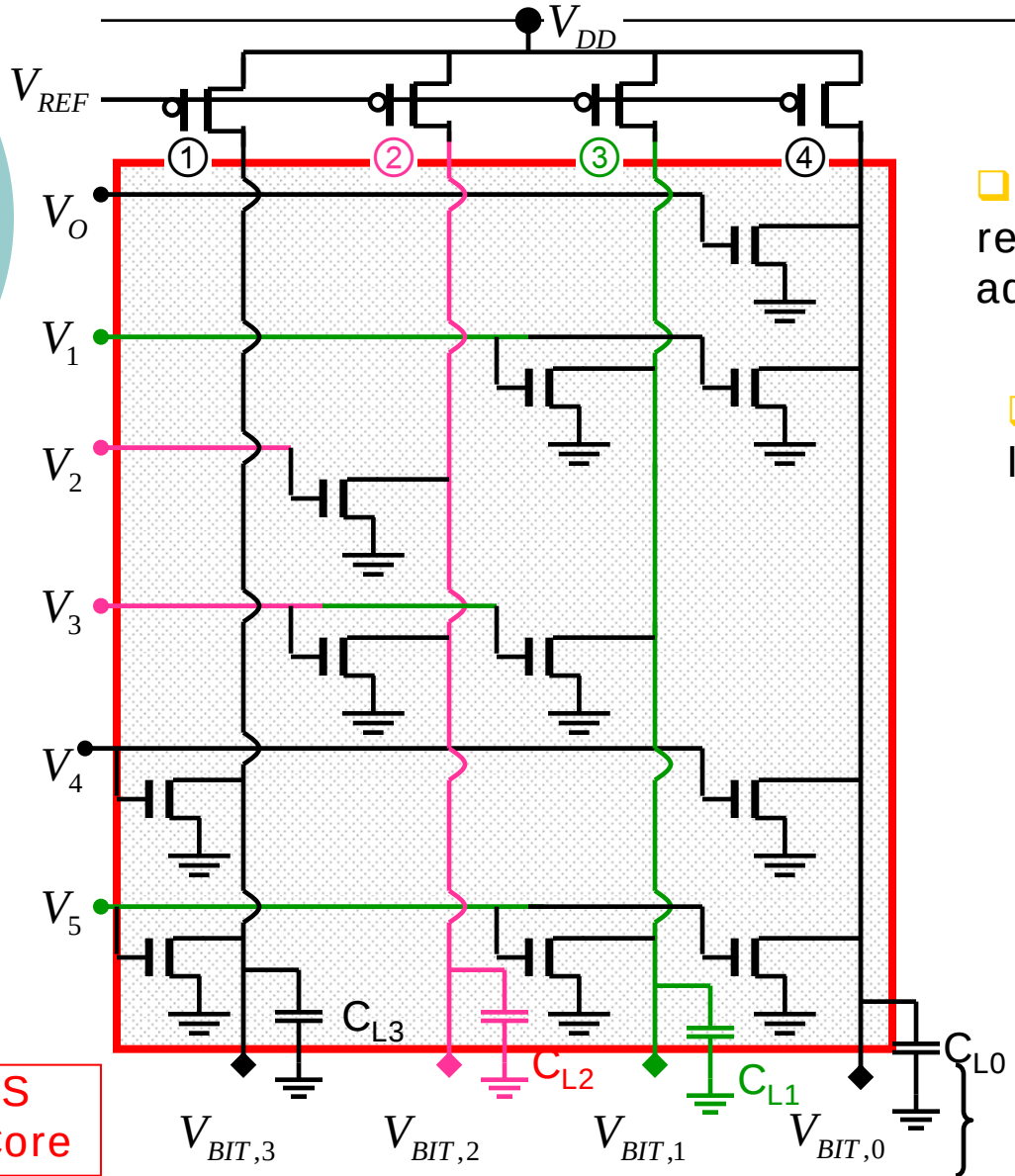
CMOS Read-Only Memories







Operation of CMOS ROM Cell



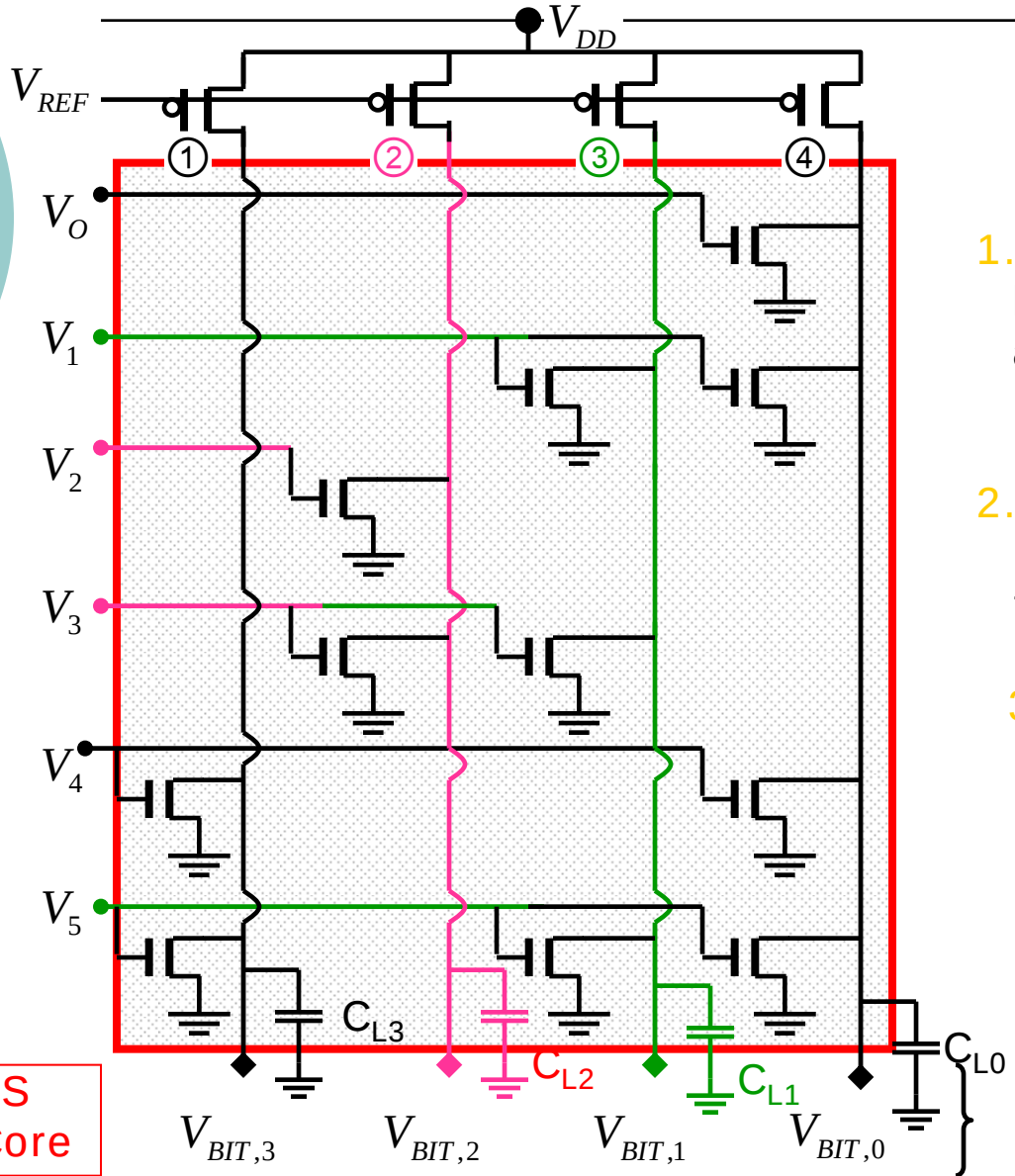
- This circuit (*CMOS ROM*) represents a simple four bit, six address ROM cell

- The data out bit lines are labeled

$V_{BIT,3}$ $V_{BIT,2}$ $V_{BIT,1}$ $V_{BIT,0}$

CMOS ROM Core

Operation of CMOS ROM Cell Precharging Holding Capacitances



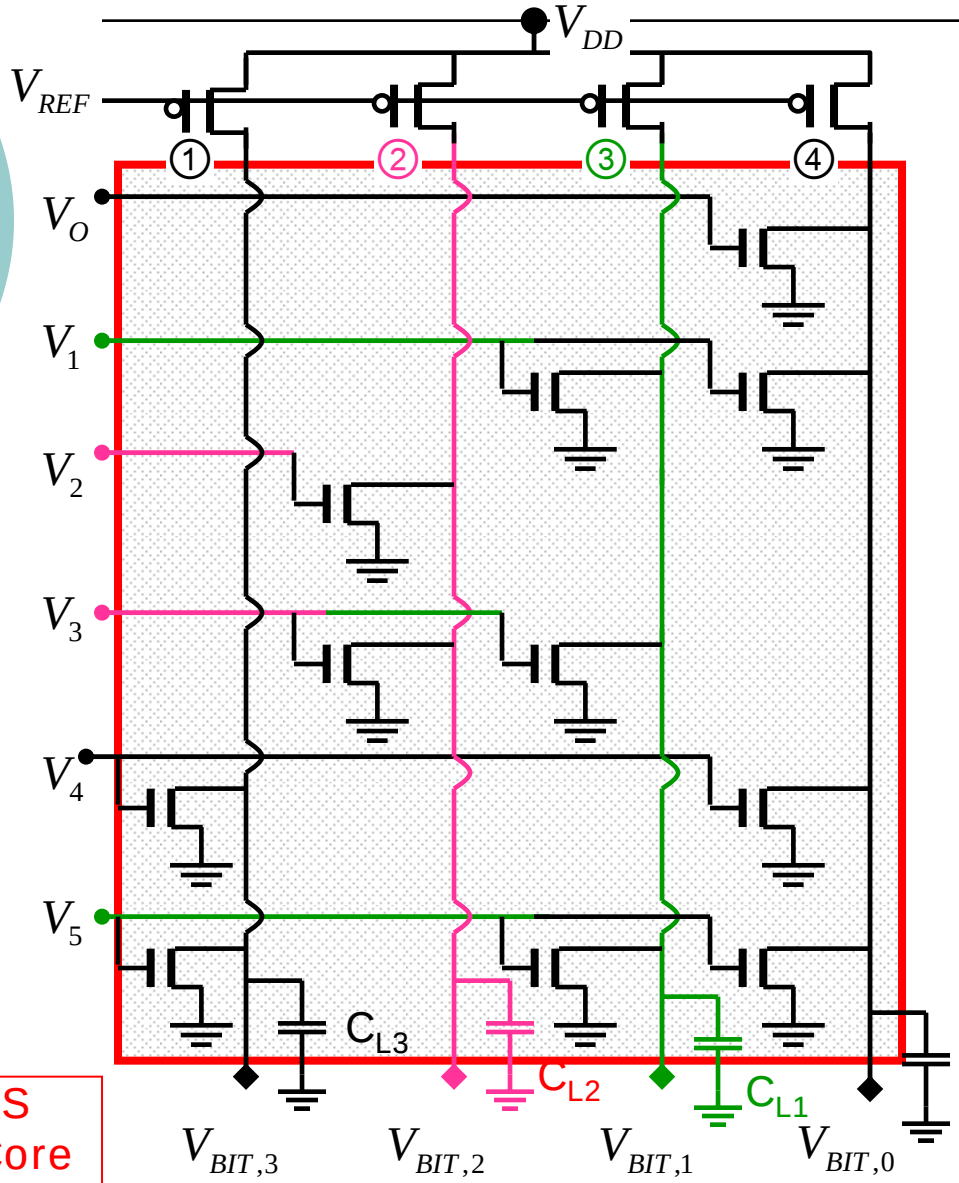
1. The V_{REF} must be temporarily low while the all the six address inputs are held low.

2. These voltages charge the holding capacitance of each of the four bit output lines

3. After all the holding capacitances have been charged to $V_{OH}=V_{DD}$, the V_{REF} is brought to high.

CMOS ROM Core

Operation of CMOS ROM Cell Precharging Holding Capacitances



$V_{REF}(Low)$

Only V_O is high "1"

Data Output values: **1110**

Only V_1 is high "1"

Data Output values: **1100**

Only V_2 is high "1"

Data Output values: **1011**

Only V_3 is high "1"

Data Output values: **1001**

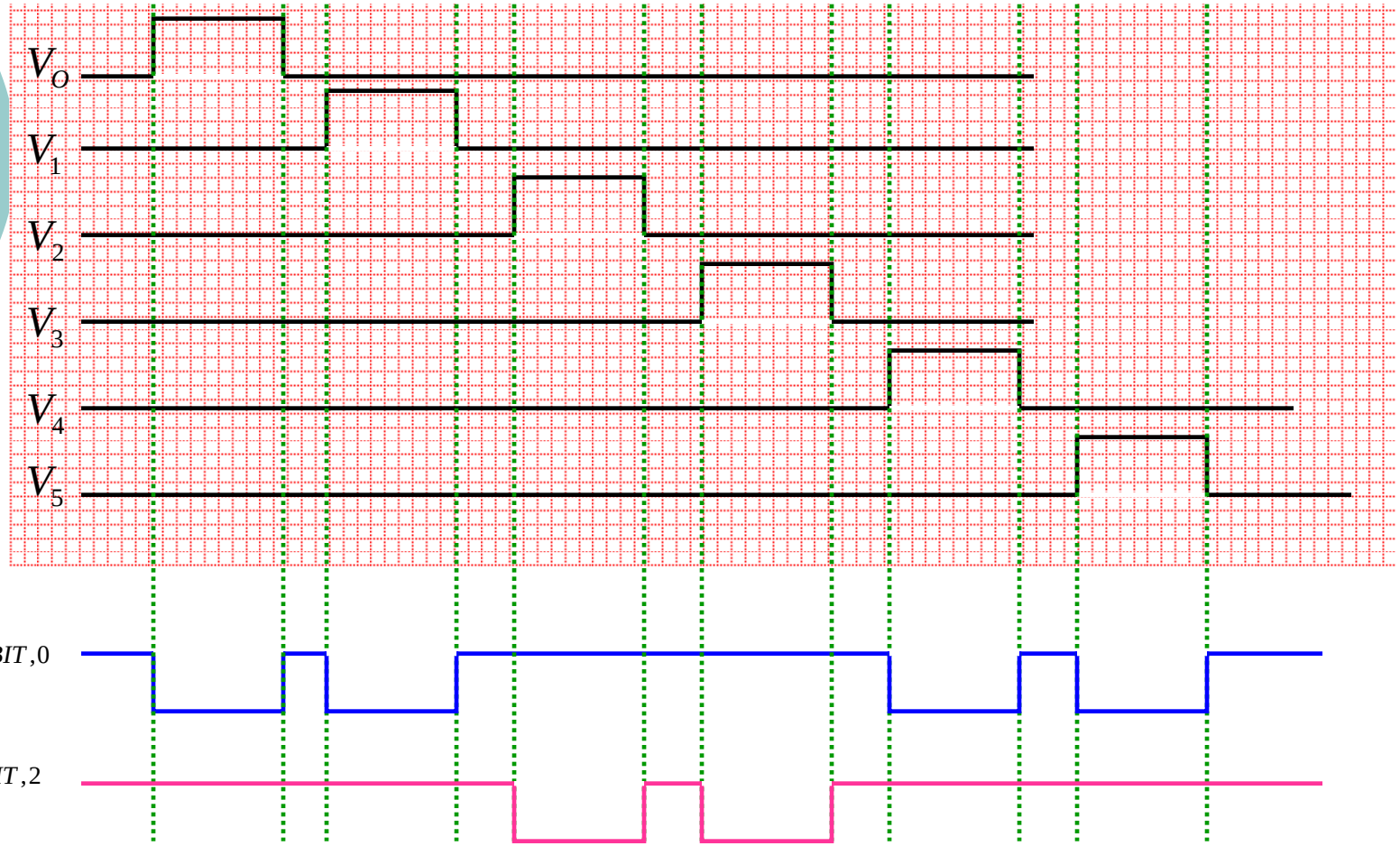
Only V_4 is high "1"

Data Output values: **0110**

Only V_5 is high "1"

Data Output values: **0100**

Utilization of CMOS ROM Cell



④: 4-input CMOS gate V_O V_1 V_4 V_5

②: 2-input CMOS gate V_2 V_3

- HW #14:Solve Problems: 32.6, 32.22, 32.27, and 32.28